command queuing engine that creates a plurality of threads of sequential commands that exist simultaneously while minimizing interrupts associated to the commands.

16. The data controller of claim 3 wherein the command queueing engine includes a transfer extend generator that generates transfer extend entries.

17. The data controller of claim 16 wherein the transfer extend generator is coupled to the buffer memory to store the transfer extend entries.

18. The data controller of claim 3 wherein the command queuing engine includes a data retrieval channel.

19. The data controller of claim 18 wherein the command queueing engine further includes a status retrieval channel.

20. The data controller of claim 18 wherein the data retrieval channel is coupled to the buffer memory to retrieve transfer extend entries and to return used read pointers.

Please add the following new claims:

21. (NEW) A data controller of a peripheral device having a storage medium and a processor, wherein the data controller minimizes interrupts to the processor by re-ordering a plurality of commands received from a host computer from an order of arrival into an order of sequence in the storage medium.

22. (NEW) The data controller of claim 21, further comprising a command queueing engine configured to arrange the plurality of commands into at least one thread.

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23. (NEW) The data controller of claim 22, wherein the command queueing engine comprises:

a transfer extend generator configured to generate transfer extend entries for a data transfer between the storage medium and a host computer; and

a data retrieval channel coupled to receive the transfer extend entries for programming the data transfer.

24. (NEW) The data controller of claim 23, wherein the command queueing engine further comprises a status retrieval channel.

25. (NEW) The data controller of claim 24, wherein each of the retrieval channels are coupled to receive transfer extend entries and to provide used read pointers to a first storage device of the peripheral device.

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26. (NEW) A peripheral device that includes a data controller, a microprocessor, a buffer memory, local memory and a storage medium, and that is couplable to a host, wherein the data controller creates threads of a plurality of commands and generates interrupts at the beginning and end of the plurality of commands relative to a data transfer.